FIG. 1

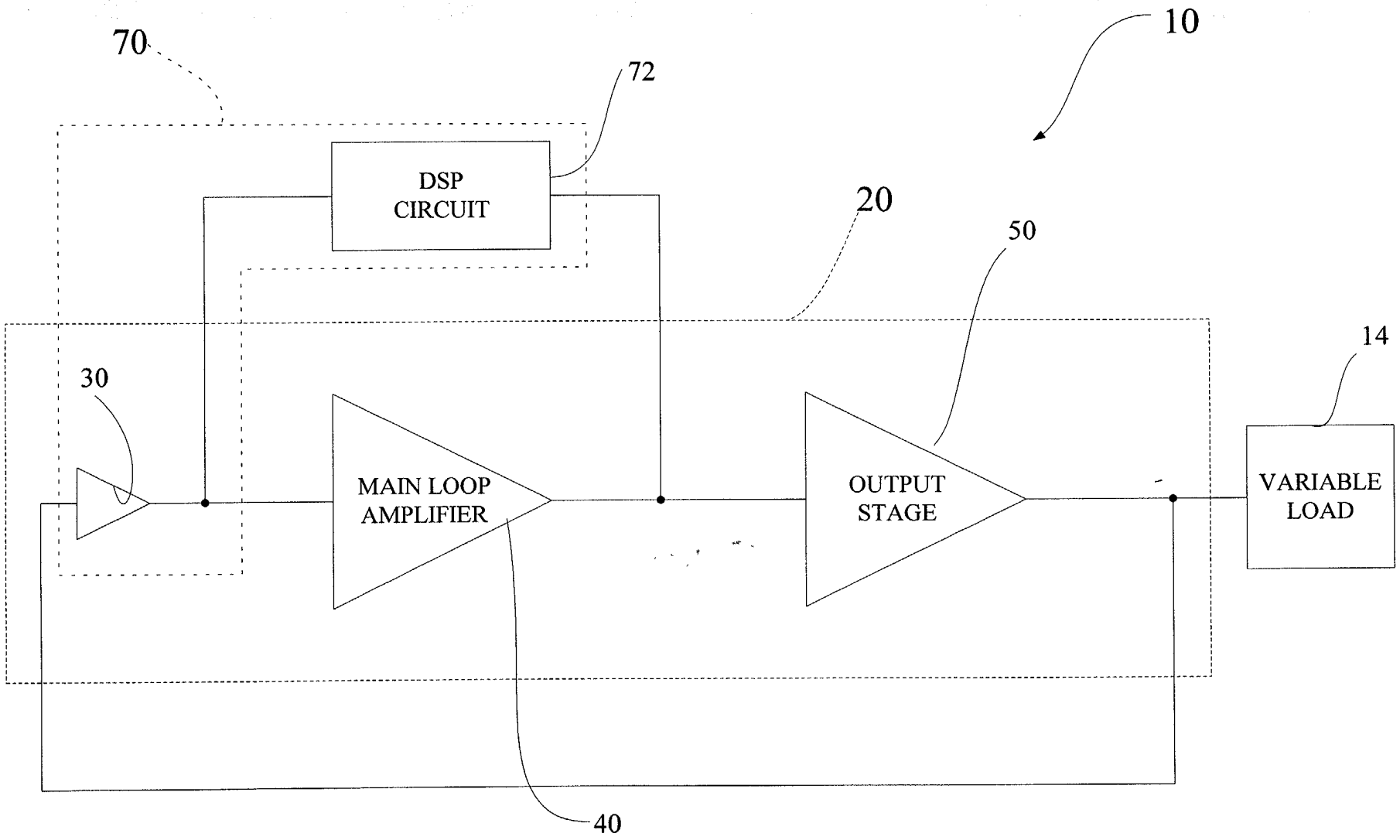
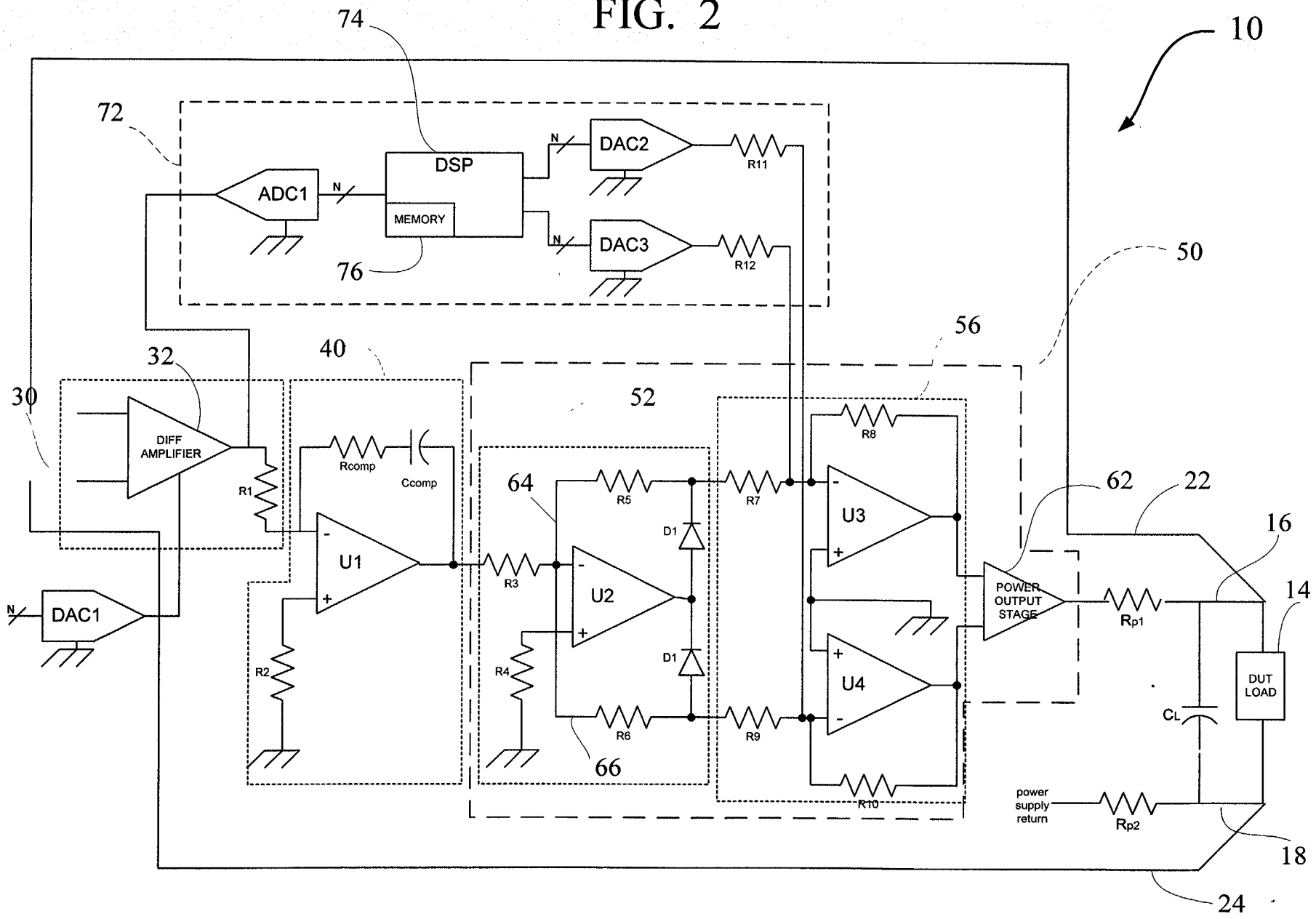

70
72
10
DSP
CIRCUIT
20
50
14
30
MAIN LOOP
AMPLIFIER
OUTPUT
STAGE
VARIABLE
LOAD
40

FIG. 2


74
10
72
DSP
ADC1
N
MEMORY
76
DAC2
DAC3
R11
R12
50
56
32
40
30
52
DIFF AMPLIFIER
R1
Rcomp
Ccomp
64
R5
R7
R8
D1
U1
U2
U3
U4
R3
R4
R6
R9
R10
R2
62
22
16
14
DAC1
POWER OUTPUT STAGE
Rp1
DUT LOAD
CL
power supply return
Rp2
18
24
66

20080730 040007

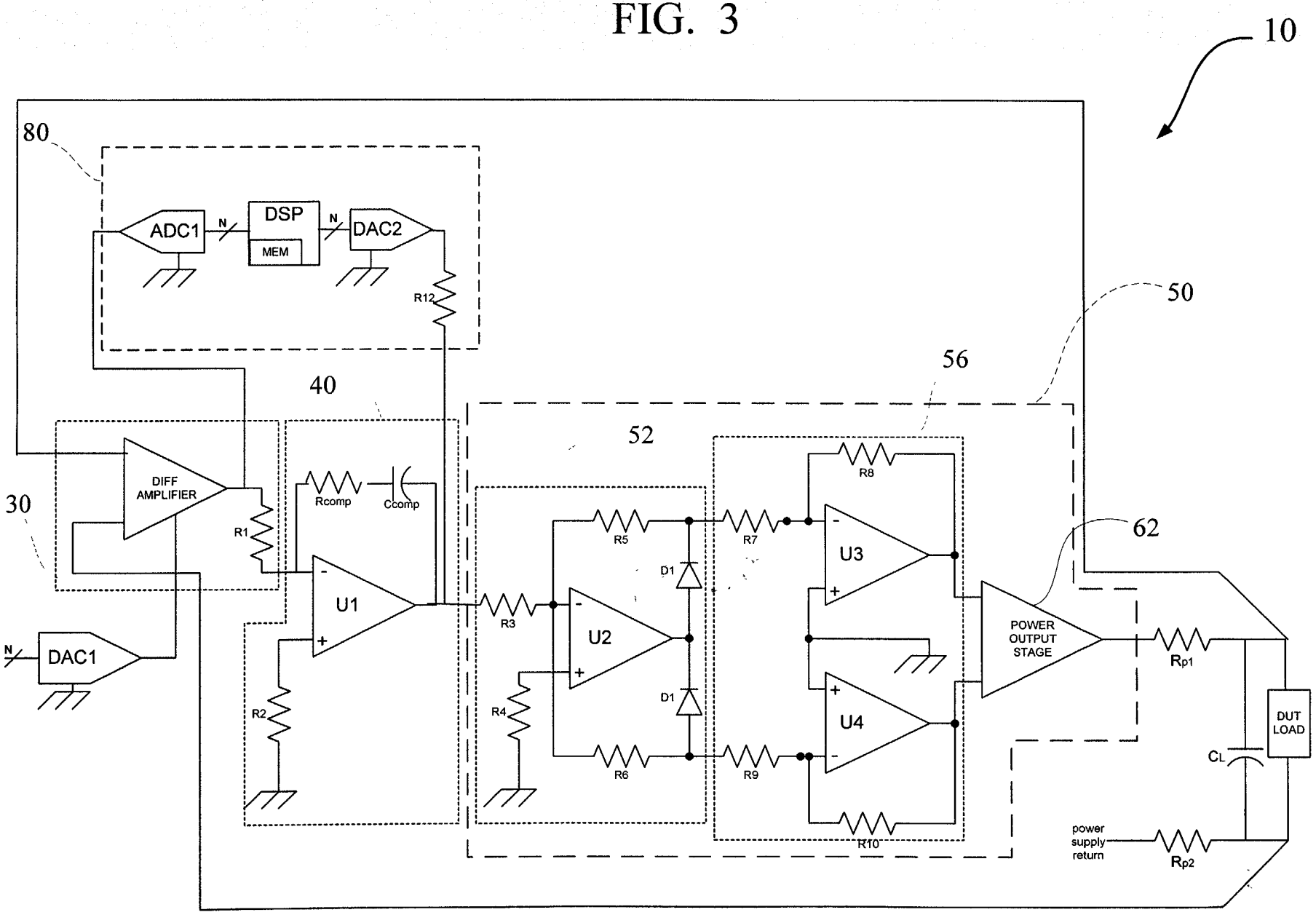



FIG. 3